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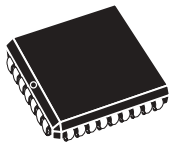
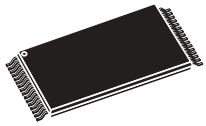
# M29F010B

## 1 Mbit (128Kb x8, Uniform Block) Single Supply Flash Memory

- SINGLE 5V±10% SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- ACCESS TIME: 45 ns
- PROGRAMMING TIME
  - 8 µs per Byte typical
- 8 UNIFORM 16 KBytes MEMORY BLOCKS
- PROGRAM/ERASE CONTROLLER
  - Embedded Byte Program algorithm
  - Embedded Multi-Block/Chip Erase algorithm
  - Status Register Polling and Toggle Bits
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1 ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: 20h
- ECOPACK® PACKAGES AVAILABLE



PLCC32 (K)



TSOP32 (N)
8 x 20mm

**Figure 1. Logic Diagram**

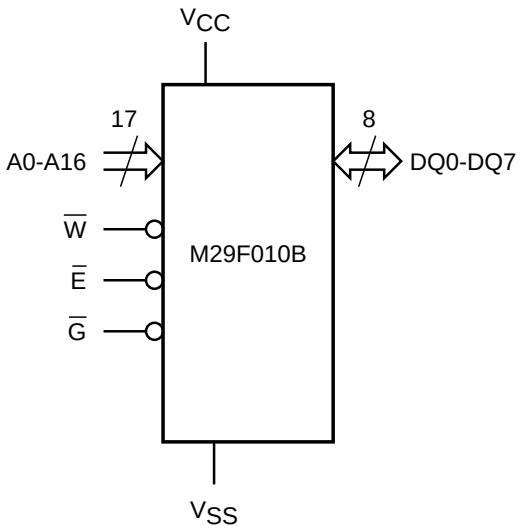


**Figure 2. PLCC Connections**

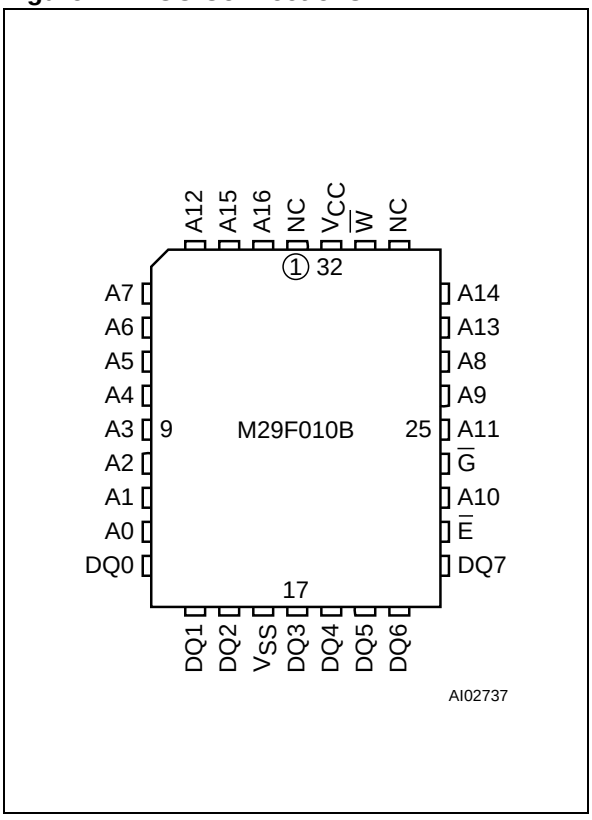



**Figure 3. TSOP Connections**

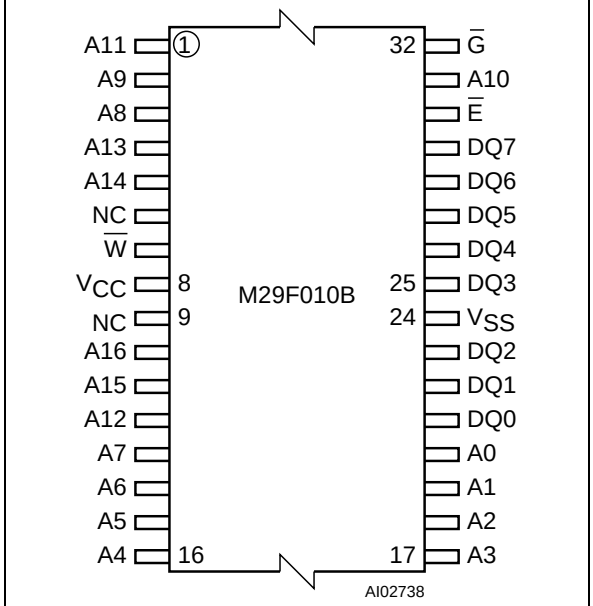



**Table 1. Signal Names**

| | |
|---|---|
| A0-A16 | Address Inputs |
| DQ0-DQ7 | Data Inputs/Outputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $V_{CC}$ | Supply Voltage |
| $V_{SS}$ | Ground |
| NC | Not Connected Internally |

**Table 2. Uniform Block Addresses, M29F010B**

| # | Size (Kbytes) | Address Range |
|---|---|---|
| 7 | 16 | 1C000h-1FFFFh |
| 6 | 16 | 18000h-1BFFFh |
| 5 | 16 | 14000h-17FFFh |
| 4 | 16 | 10000h-13FFFh |
| 3 | 16 | 0C000h-0FFFFh |
| 2 | 16 | 08000h-0BFFFh |
| 1 | 16 | 04000h-07FFFh |
| 0 | 16 | 00000h-03FFFh |

**Table 3. Absolute Maximum Ratings (1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $T_A$ | Ambient Operating Temperature (Temperature Range Option 1) | 0 to 70 | °C |
| | Ambient Operating Temperature (Temperature Range Option 6) | –40 to 85 | °C |
| | Ambient Operating Temperature (Temperature Range Option 3) | –40 to 125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –50 to 125 | °C |
| $T_{STG}$ | Storage Temperature | –65 to 150 | °C |
| $V_{IO}$ (2) | Input or Output Voltage | –0.6 to 6 | V |
| $V_{CC}$ | Supply Voltage | –0.6 to 6 | V |
| $V_{ID}$ | Identification Voltage | –0.6 to 13.5 | V |

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns during transitions.

## SUMMARY DESCRIPTION

The M29F010B is a 1 Mbit (128Kb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single 5V supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in PLCC32, TSOP32 (8 x 20mm) packages and it is supplied with all the bits erased (set to '1').

In order to meet environmental requirements, ST offers the M29F010B in ECOPACK® packages. ECOPACK packages are Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

## SIGNAL DESCRIPTIONS

See Figure 1, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

**Address Inputs (A0-A16).** The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

**Data Inputs/Outputs (DQ0-DQ7).** The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

**Chip Enable ($\overline{E}$).** The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, $V_{IH}$, all other pins are ignored.

**Output Enable ($\overline{G}$).** The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

**Write Enable ($\overline{W}$).** The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

**$V_{CC}$ Supply Voltage.** The $V_{CC}$ Supply Voltage supplies the power for all operations (Read, Program, Erase etc.).

The Command Interface is disabled when the $V_{CC}$ Supply Voltage is less than the Lockout Voltage,

$V_{LKO}$. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/ Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the $V_{CC}$ Supply Voltage pin and the $V_{SS}$ Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, $I_{CC4}$.

**Vss Ground.** The $V_{SS}$ Ground is the reference for all voltage measurements.

## BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See Table 4, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

**Bus Read.** Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, $V_{IL}$, to Chip Enable and Output Enable and keeping Write Enable High, $V_{IH}$. The Data Inputs/Outputs will output the value, see Figure 8, Read Mode AC Waveforms, and Table 11, Read AC Characteristics, for details of when the output becomes valid.

**Bus Write.** Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, $V_{IH}$, during the whole Bus Write operation. See Figures 9 and 10, Write AC Waveforms, and Tables 12 and 13, Write AC Characteristics, for details of the timing requirements.

**Output Disable.** The Data Inputs/Outputs are in the high impedance state when Output Enable is High, $V_{IH}$.

**Standby.** When Chip Enable is High, $V_{IH}$, the Data Inputs/Outputs pins are placed in the high-impedance state and the Supply Current is reduced to the Standby level.

When Chip Enable is at $V_{IH}$ the Supply Current is reduced to the TTL Standby Supply Current $I_{CC2}$. To further reduce the Supply Current to the CMOS Standby Supply Current, $I_{CC3}$, Chip Enable should be held within $V_{CC}$ ± 0.2V. For Standby current levels see Table 10, DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, $I_{CC4}$, for Program or Erase operations until the operation completes.

**Automatic Standby.** If CMOS levels ($V_{CC}$ ± 0.2V) are used to drive the bus and the bus is inactive for 150ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the CMOS Standby Supply Current, $I_{CC3}$. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

### Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require $V_{ID}$ to be applied to some pins.

**Electronic Signature.** The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Table 4, Bus Operations.

**Block Protection** and **Blocks Unprotection.** Each block can be separately protected against accidental Program or Erase. Protected blocks can be unprotected to allow data to be changed. Block Protection and Blocks Unprotection operations must only be performed on programming equipment. For further information refer to Application Note AN1122, Applying Protection and Unprotection to M29 Series Flash.

**Table 4. Bus Operations**

| Operation | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | Address Inputs | Data Inputs/Outputs |
|---|---|---|---|---|---|
| Bus Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | Cell Address | Data Output |
| Bus Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | Command Address | Data Input |
| Output Disable | X | $V_{IH}$ | $V_{IH}$ | X | Hi-Z |
| Standby | $V_{IH}$ | X | X | X | Hi-Z |
| Read Manufacturer Code | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | A0 = $V_{IL}$, A1 = $V_{IL}$, A9 = $V_{ID}$, Others $V_{IL}$ or $V_{IH}$ | 20h |
| Read Device Code | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | A0 = $V_{IH}$, A1 = $V_{IL}$, A9 = $V_{ID}$, Others $V_{IL}$ or $V_{IH}$ | 20h |

Note: X = $V_{IL}$ or $V_{IH}$.

## COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

The commands are summarized in Table 5, Commands. Refer to Table 5 in conjunction with the text descriptions below.

**Read/Reset Command.** The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

If the Read/Reset command is issued during a Block Erase operation or following a Programming or Erase error then the memory will take upto 10µs to abort. During the abort period no valid data can be read from the memory. Issuing a Read/Reset command during a Block Erase operation will leave invalid data in the memory.

**Auto Select Command.** The Auto Select command is used to read the Manufacturer Code, the Device Code and the Block Protection Status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until another command is issued.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = $V_{IL}$ and A1 = $V_{IL}$. The other address bits may be set to either $V_{IL}$ or $V_{IH}$. The Manufacturer Code for STMicroelectronics is 20h.

The Device Code can be read using a Bus Read operation with A0 = $V_{IH}$ and A1 = $V_{IL}$. The other address bits may be set to either $V_{IL}$ or $V_{IH}$. The Device Code for the M29F010B is 20h.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = $V_{IL}$, A1 = $V_{IH}$, and A14-A16 specifying the address of the block. The other address bits may be set to either $V_{IL}$ or $V_{IH}$. If the addressed block is protected then 01h is output on the Data Inputs/Outputs, otherwise 00h is output.

**Program Command.** The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 6. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Com-

mands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

**Unlock Bypass Command.** The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

**Unlock Bypass Program Command.** The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. A protected block cannot be programmed; the operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass Mode. See the Program command for details on the behavior.

**Unlock Bypass Reset Command.** The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command.

**Chip Erase Command.** The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 6. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to '1'. All previous data is lost.

**Block Erase Command.** The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller about 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend and Read/Reset commands. Typical block erase times are given in Table 6. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Block Erase Command sets all of the bits in the unprotected selected blocks to '1'. All previous data in the selected blocks is lost.

**Erase Suspend Command.** The Erase Suspend Command may be used to temporarily suspend a

Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within 15µs of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It will not be possible to select any further blocks for erasure after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. Reading from blocks that are being erased will output the Status Register. It is also possible to enter the Auto Select mode: the memory will behave as in the Auto Select mode on all blocks until a Read/Reset command returns the memory to Erase Suspend mode.

**Erase Resume Command.** The Erase Resume command must be used to restart the Program/Erase Controller from Erase Suspend. An erase can be suspended and resumed more than once.

**Table 5. Commands**

| Command | Length | Bus Write Operations | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1st | | 2nd | | 3rd | | 4th | | 5th | | 6th | |
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read/Reset | 1 | X | F0 | | | | | | | | | | |
| | 3 | 555 | AA | 2AA | 55 | X | F0 | | | | | | |
| Auto Select | 3 | 555 | AA | 2AA | 55 | 555 | 90 | | | | | | |
| Program | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| Unlock Bypass | 3 | 555 | AA | 2AA | 55 | 555 | 20 | | | | | | |
| Unlock Bypass Program | 2 | X | A0 | PA | PD | | | | | | | | |
| Unlock Bypass Reset | 2 | X | 90 | X | 00 | | | | | | | | |
| Chip Erase | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| Block Erase | 6+ | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | BA | 30 |
| Erase Suspend | 1 | X | B0 | | | | | | | | | | |
| Erase Resume | 1 | X | 30 | | | | | | | | | | |

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block.

All values in the table are in hexadecimal.

The Command Interface only uses address bits A0-A10 to verify the commands, the upper address bits are Don't Care.

**Read/Reset.** After a Read/Reset command, read the memory as normal until another command is issued.

**Auto Select.** After an Auto Select command, read Manufacturer ID, Device ID or Block Protection Status.

**Program, Unlock Bypass Program, Chip Erase, Block Erase.** After these commands read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode. Add additional Blocks during Block Erase Command with additional Bus Write Operations until the Timeout Bit is set.

**Unlock Bypass.** After the Unlock Bypass command issue Unlock Bypass Program or Unlock Bypass Reset commands.

**Unlock Bypass Reset.** After the Unlock Bypass Reset command read the memory as normal until another command is issued.

**Erase Suspend.** After the Erase Suspend command read non-erasing memory blocks as normal, issue Auto Select and Program commands on non-erasing blocks as normal.

**Erase Resume.** After the Erase Resume command the suspended Erase operation resumes, read the Status Register until the Program/Erase Controller completes and the memory returns to Read Mode.

**Table 6. Program, Erase Times and Program, Erase Endurance Cycles**
($T_A$ = 0 to 70°C, –40 to 85°C or –40 to 125°C)

| Parameter | Min | Typ(1) | Typical after 100k W/E Cycles(1) | Max | Unit |
|---|---|---|---|---|---|
| Chip Erase (All bits in the memory set to '0') | | 0.6 | 0.6 | | sec |
| Chip Erase | | 1.3 | 1.3 | 6 | sec |
| Block Erase (16 Kbytes) | | 0.3 | 0.3 | 2 | sec |
| Program | | 8 | 8 | 150 | µs |
| Chip Program | | 1.2 | 1.2 | 4.5 | sec |
| Program/Erase Cycles (per Block) | 100,000 | | | | cycles |

Note: 1. $T_A$ = 25°C, $V_{CC}$ = 5V.

## STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in Table 7, Status Register Bits.

**Data Polling Bit (DQ7).** The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a '1' during a Bus Read operation within a block being erased. The Data Polling Bit will change from a '0' to a '1' when the Program/Erase Controller has suspended the Erase operation.

Figure 4, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

**Toggle Bit (DQ6).** The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

Figure 5, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

**Error Bit (DQ5).** The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set at '0' back to '1' and attempting to do so may or may not set DQ5 at '1'. In both cases, a successive Bus Read operation will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

**Erase Timer Bit (DQ3).** The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to '1'. Before the Program/Erase Controller starts the Erase Timer Bit is set to '0' and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.

**Alternative Toggle Bit (DQ2).** The Alternative Toggle Bit can be used to monitor the Program/

Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations from addresses within the blocks being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

**Table 7. Status Register Bits**

| Operation | Address | DQ7 | DQ6 | DQ5 | DQ3 | DQ2 |
|---|---|---|---|---|---|---|
| Program | Any Address | $\overline{DQ7}$ | Toggle | 0 | – | – |
| Program During Erase Suspend | Any Address | $\overline{DQ7}$ | Toggle | 0 | – | – |
| Program Error | Any Address | $\overline{DQ7}$ | Toggle | 1 | – | – |
| Chip Erase | Any Address | 0 | Toggle | 0 | 1 | Toggle |
| Block Erase before timeout | Erasing Block | 0 | Toggle | 0 | 0 | Toggle |
| | Non-Erasing Block | 0 | Toggle | 0 | 0 | No Toggle |
| Block Erase | Erasing Block | 0 | Toggle | 0 | 1 | Toggle |
| | Non-Erasing Block | 0 | Toggle | 0 | 1 | No Toggle |
| Erase Suspend | Erasing Block | 1 | No Toggle | 0 | – | Toggle |
| | Non-Erasing Block | Data read as normal | | | | |
| Erase Error | Good Block Address | 0 | Toggle | 1 | 1 | No Toggle |
| | Faulty Block Address | 0 | Toggle | 1 | 1 | Toggle |

Note: Unspecified data bits should be ignored.

**Figure 4. Data Polling Flowchart**

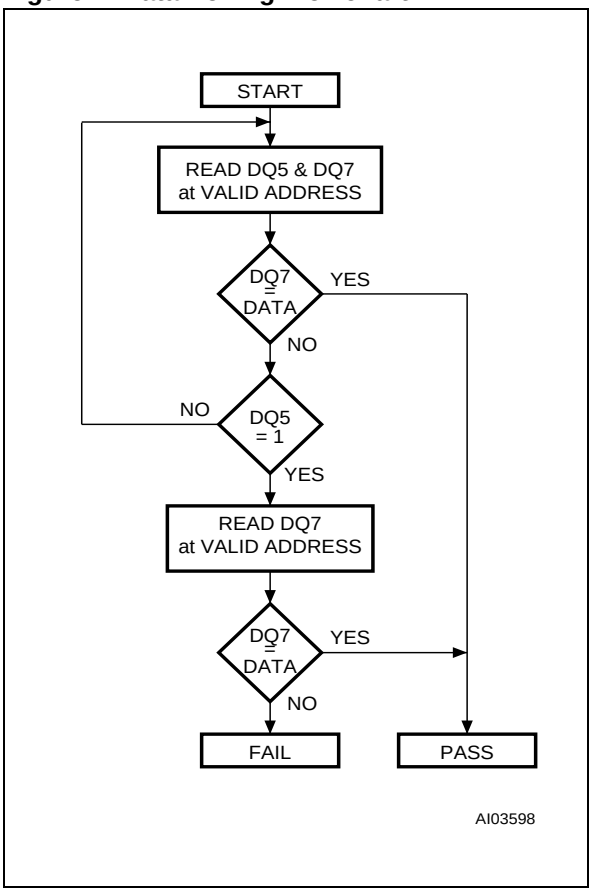



**Figure 5. Data Toggle Flowchart**

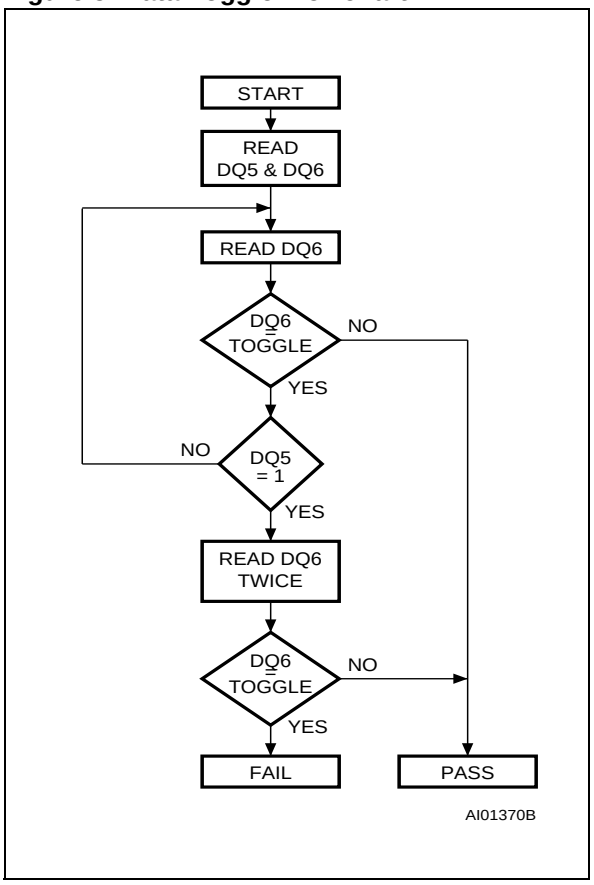


**Table 8. AC Measurement Conditions**

| Parameter | M29F010B | |
|---|---|---|
| | 45 | 70 / 90 / 120 |
| AC Test Conditions | High Speed | Standard |
| Load Capacitance ($C_L$) | 30pF | 100pF |
| Input Rise and Fall Times | ≤10ns | ≤10ns |
| Input Pulse Voltages | 0 to 3V | 0.45 to 2.4V |
| Input and Output Timing Ref. Voltages | 1.5V | 0.8V and 2V |

**Figure 6. AC Testing Input Output Waveform**

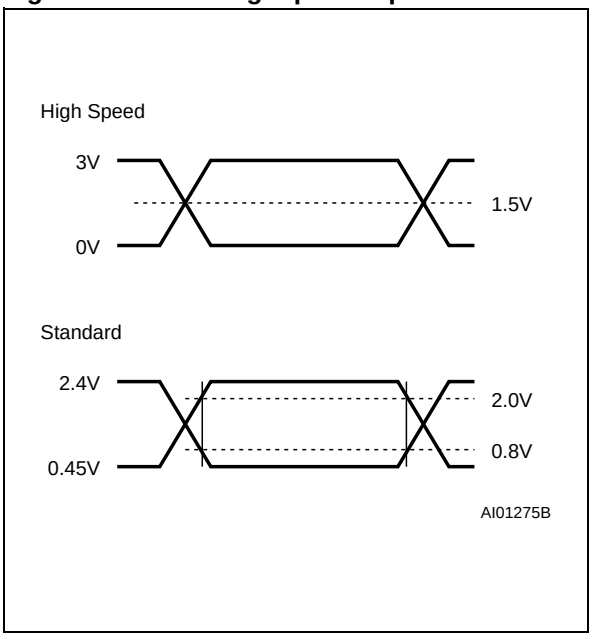



**Figure 7. AC Testing Load Circuit**

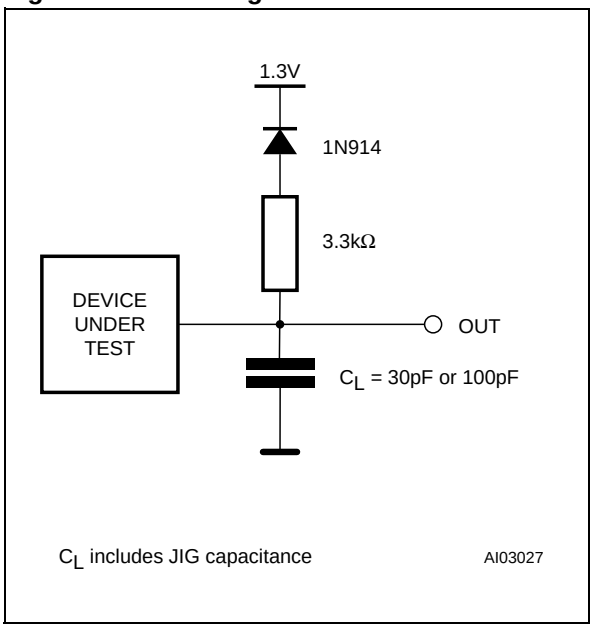



**Table 9. Capacitance**
($T_A$ = 25 °C, f = 1 MHz)

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | | 12 | pF |

Note: Sampled only, not 100% tested.

**Table 10. DC Characteristics**
($T_A$ = 0 to 70°C, –40 to 85°C or –40 to 125°C)

| Symbol | Parameter | Test Condition | Min | Typ (2) | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current | $0V \le V_{IN} \le V_{CC}$ | | | ±1 | µA |
| $I_{LO}$ | Output Leakage Current | $0V \le V_{OUT} \le V_{CC}$ | | | ±1 | µA |
| $I_{CC1}$ | Supply Current (Read) | $\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz | | 5 | 15 | mA |
| $I_{CC2}$ | Supply Current (Standby) TTL | $\overline{E} = V_{IH}$ | | | 1 | mA |
| $I_{CC3}$ | Supply Current (Standby) CMOS | $\overline{E} = V_{CC}$ ±0.2V | | 30 | 100 | µA |
| $I_{CC4}$ (1) | Supply Current (Program/Erase) | Program/Erase Controller active | | | 20 | mA |
| $V_{IL}$ | Input Low Voltage | | –0.5 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2 | | $V_{CC}$ +0.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 5.8mA | | | 0.45 | V |
| $V_{OH}$ | Output High Voltage TTL | $I_{OH}$ = –2.5mA | 2.4 | | | V |
| | Output High Voltage CMOS | $I_{OH}$ = –100µA | $V_{CC}$ –0.4 | | | V |
| $V_{ID}$ | Identification Voltage | | 11.5 | | 12.5 | V |
| $I_{ID}$ | Identification Current | $A9 = V_{ID}$ | | | 100 | µA |
| $V_{LKO}$ (1) | Program/Erase Lockout Supply Voltage | | 3.2 | | 4.2 | V |

Note: 1. Sampled only, not 100% tested.
2. $T_A$ = 25°, $V_{CC}$ = 5V.

**Table 11. Read AC Characteristics**
(TA = 0 to 70°C, –40 to 85°C or –40 to 125°C)

| Symbol | Alt | Parameter | Test Condition | | M29F010B | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | 45 | 70 / 90 / 120 | |
| $t_{AVAV}$ | $t_{RC}$ | Address Valid to Next Address Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | Min | 45 | 70 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address Valid to Output Valid | $\overline{E}$ = $V_{IL}$, $\overline{G}$ = $V_{IL}$ | Max | 45 | 70 | ns |
| $t_{ELQX}$ (1) | $t_{LZ}$ | Chip Enable Low to Output Transition | $\overline{G}$ = $V_{IL}$ | Min | 0 | 0 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable Low to Output Valid | $\overline{G}$ = $V_{IL}$ | Max | 45 | 70 | ns |
| $t_{GLQX}$ (1) | $t_{OLZ}$ | Output Enable Low to Output Transition | $\overline{E}$ = $V_{IL}$ | Min | 0 | 0 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable Low to Output Valid | $\overline{E}$ = $V_{IL}$ | Max | 25 | 30 | ns |
| $t_{EHQZ}$ (1) | $t_{HZ}$ | Chip Enable High to Output Hi-Z | $\overline{G}$ = $V_{IL}$ | Max | 15 | 20 | ns |
| $t_{GHQZ}$ (1) | $t_{DF}$ | Output Enable High to Output Hi-Z | $\overline{E}$ = $V_{IL}$ | Max | 15 | 20 | ns |
| $t_{EHQX}$ $t_{GHQX}$ $t_{AXQX}$ | $t_{OH}$ | Chip Enable, Output Enable or Address Transition to Output Transition | | Min | 0 | 0 | ns |

Note: 1. Sampled only, not 100% tested.

**Figure 8. Read Mode AC Waveforms**

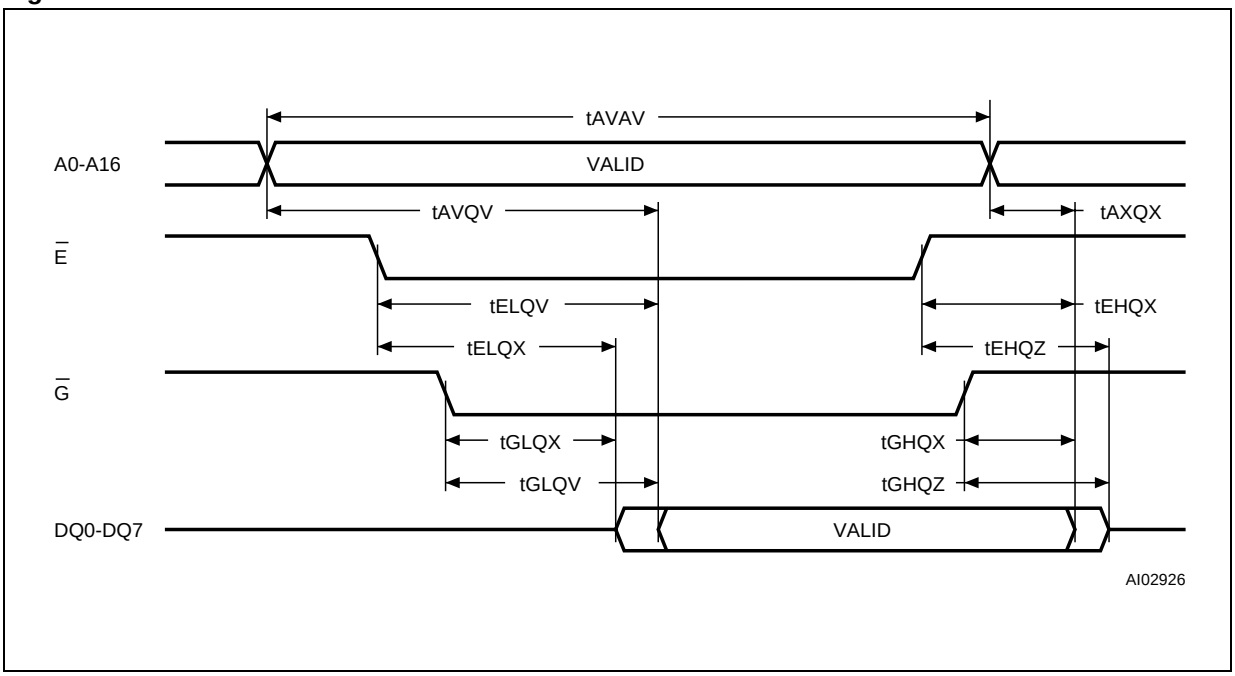


**Table 12. Write AC Characteristics, Write Enable Controlled**
($T_A$ = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

| Symbol | Alt | Parameter | | M29F010B | | Unit |
|---|---|---|---|---|---|---|
| | | | | 45 | 70 / 90 / 120 | |
| $t_{AVAV}$ | $t_{WC}$ | Address Valid to Next Address Valid | Min | 45 | 70 | ns |
| $t_{ELWL}$ | $t_{CS}$ | Chip Enable Low to Write Enable Low | Min | 0 | 0 | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Enable Low to Write Enable High | Min | 40 | 45 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Input Valid to Write Enable High | Min | 25 | 30 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Write Enable High to Input Transition | Min | 0 | 0 | ns |
| $t_{WHEH}$ | $t_{CH}$ | Write Enable High to Chip Enable High | Min | 0 | 0 | ns |
| $t_{WHWL}$ | $t_{WPH}$ | Write Enable High to Write Enable Low | Min | 20 | 20 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Valid to Write Enable Low | Min | 0 | 0 | ns |
| $t_{WLAX}$ | $t_{AH}$ | Write Enable Low to Address Transition | Min | 40 | 45 | ns |
| $t_{GHWL}$ | | Output Enable High to Write Enable Low | Min | 0 | 0 | ns |
| $t_{WHGL}$ | $t_{OEH}$ | Write Enable High to Output Enable Low | Min | 0 | 0 | ns |
| $t_{VCHEL}$ | $t_{VCS}$ | $V_{CC}$ High to Chip Enable Low | Min | 50 | 50 | µs |

**Figure 9. Write AC Waveforms, Write Enable Controlled**

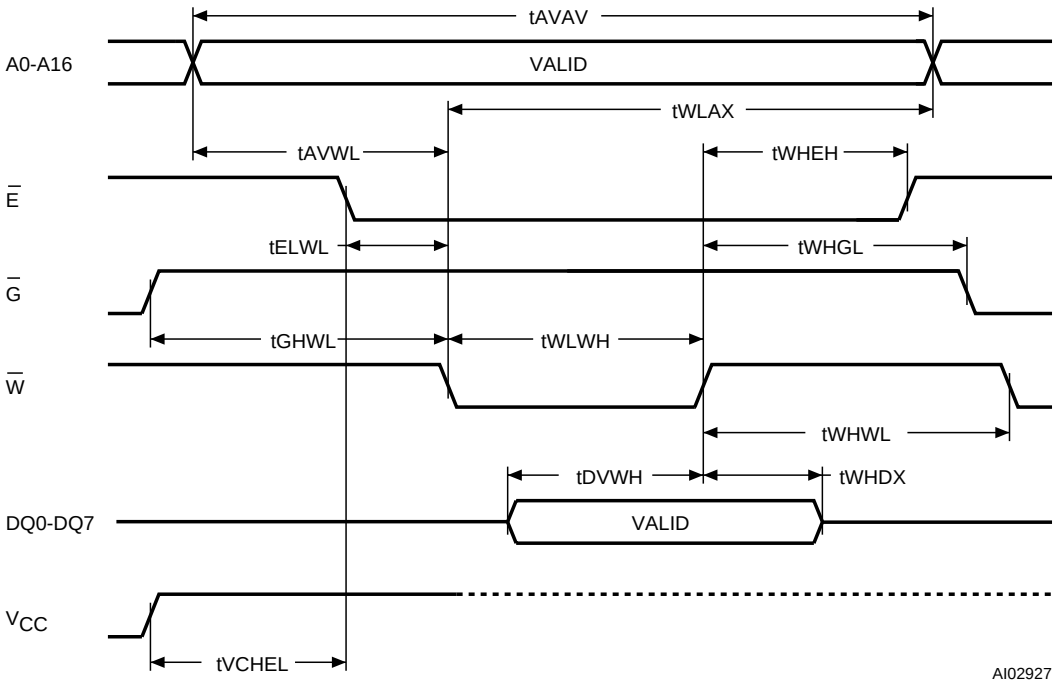


**Table 13. Write AC Characteristics, Chip Enable Controlled**
($T_A$ = 0 to 70 °C, –40 to 85 °C or –40 to 125 °C)

| Symbol | Alt | Parameter | | M29F010B | | Unit |
|---|---|---|---|---|---|---|
| | | | | 45 | 70 / 90 / 120 | |
| $t_{AVAV}$ | $t_{WC}$ | Address Valid to Next Address Valid | Min | 45 | 70 | ns |
| $t_{WLEL}$ | $t_{WS}$ | Write Enable Low to Chip Enable Low | Min | 0 | 0 | ns |
| $t_{ELEH}$ | $t_{CP}$ | Chip Enable Low to Chip Enable High | Min | 40 | 45 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Input Valid to Chip Enable High | Min | 25 | 30 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Chip Enable High to Input Transition | Min | 0 | 0 | ns |
| $t_{EHWH}$ | $t_{WH}$ | Chip Enable High to Write Enable High | Min | 0 | 0 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | Chip Enable High to Chip Enable Low | Min | 20 | 20 | ns |
| $t_{AVEL}$ | $t_{AS}$ | Address Valid to Chip Enable Low | Min | 0 | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Chip Enable Low to Address Transition | Min | 40 | 45 | ns |
| $t_{GHEL}$ | | Output Enable High Chip Enable Low | Min | 0 | 0 | ns |
| $t_{EHGL}$ | $t_{OEH}$ | Chip Enable High to Output Enable Low | Min | 0 | 0 | ns |
| $t_{VCHWL}$ | $t_{VCS}$ | $V_{CC}$ High to Write Enable Low | Min | 50 | 50 | µs |

**Figure 10. Write AC Waveforms, Chip Enable Controlled**

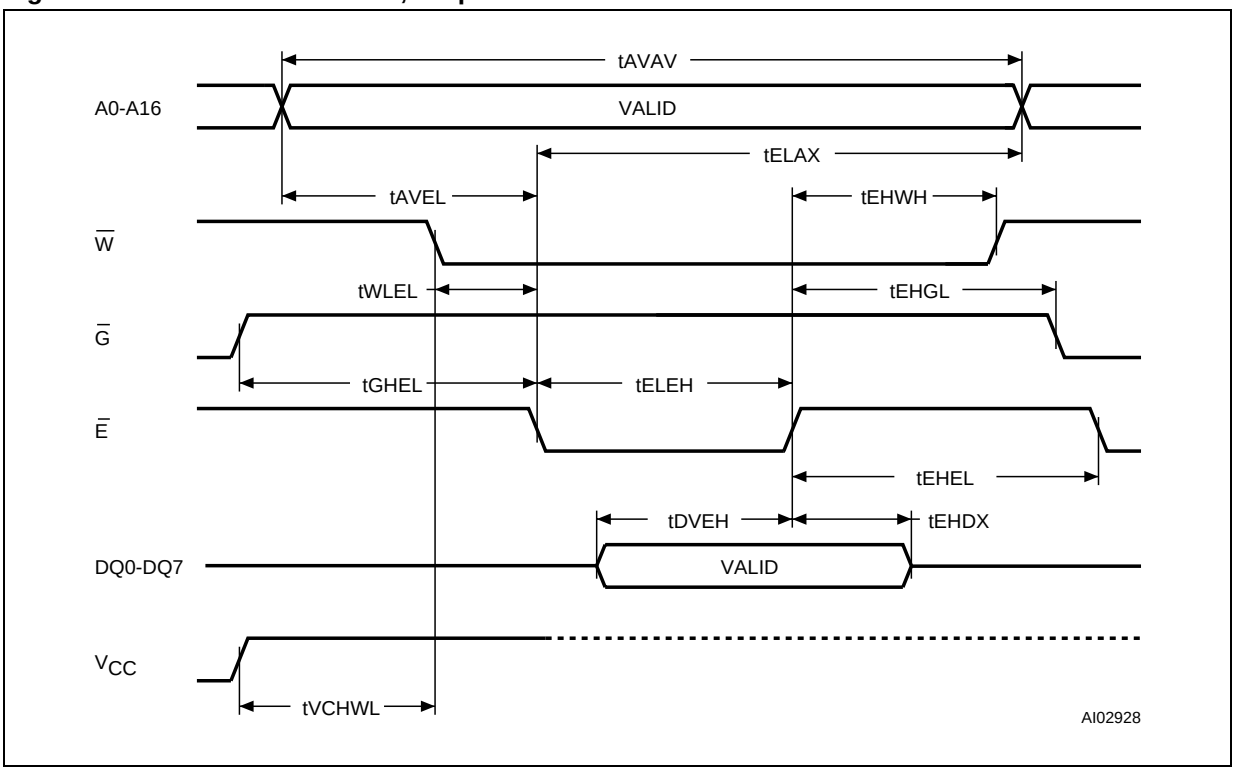


**Table 14. Ordering Information Scheme**

Example: M29F010B 70 N 1 T

**Device Type**
M29

**Operating Voltage**
F = $V_{CC}$ = 5V ± 10%

**Device Function**
010B = 1 Mbit (128Kb x8), Uniform Block

**Speed**
45 = 45 ns
70 = 70 ns
90 = 90 ns
120 = 120ns

**Package**
K = PLCC32
N = TSOP32: 8 x 20 mm

**Temperature Range**
1 = 0 to 70 °C
3 = –40 to 125 °C
6 = –40 to 85 °C

**Option**
Blank = Standard Packing
T = Tape & Reel Packing
E = ECOPACK Package, Standard Packing
F = ECOPACK Package, Tape & Reel Packing

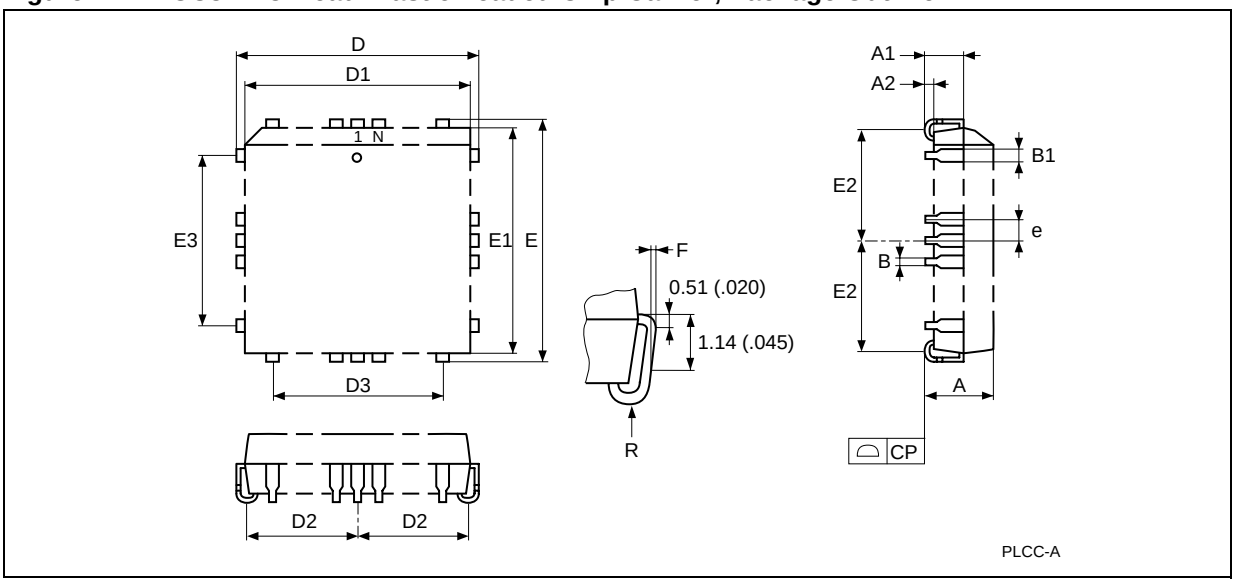
Note: The last two characters of the ordering code may be replaced by a letter code for preprogrammed parts, otherwise devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

**Table 16. PLCC32 – 32 lead Plastic Leaded Chip Carrier, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | 3.18 | 3.56 | | 0.125 | 0.140 |
| A1 | | 1.53 | 2.41 | | 0.060 | 0.095 |
| A2 | | 0.38 | – | | 0.015 | – |
| B | | 0.33 | 0.53 | | 0.013 | 0.021 |
| B1 | | 0.66 | 0.81 | | 0.026 | 0.032 |
| CP | | | 0.10 | | | 0.004 |
| D | | 12.32 | 12.57 | | 0.485 | 0.495 |
| D1 | | 11.35 | 11.51 | | 0.447 | 0.453 |
| D2 | | 4.78 | 5.66 | | 0.188 | 0.223 |
| D3 | 7.62 | – | – | 0.300 | – | – |
| E | | 14.86 | 15.11 | | 0.585 | 0.595 |
| E1 | | 13.89 | 14.05 | | 0.547 | 0.553 |
| E2 | | 6.05 | 6.93 | | 0.238 | 0.273 |
| E3 | 10.16 | – | – | 0.400 | – | – |
| e | 1.27 | – | – | 0.050 | – | – |
| F | | 0.00 | 0.13 | | 0.000 | 0.005 |
| N | | 32 | | | 32 | |
| R | 0.89 | – | – | 0.035 | – | – |

**Figure 11. PLCC32 – 32 lead Plastic Leaded Chip Carrier, Package Outline**

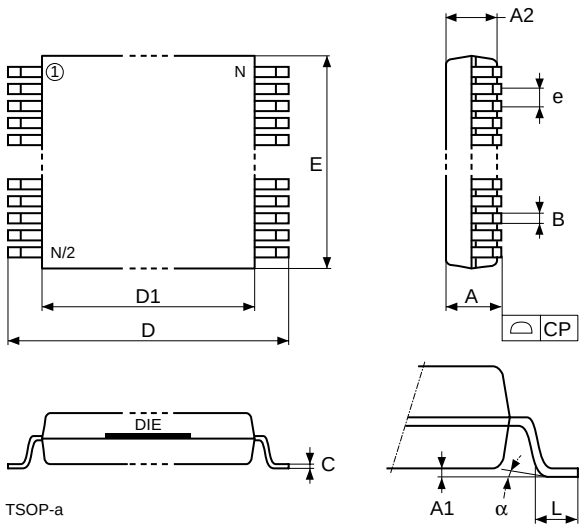



Note: Drawing is not to scale.

**Table 17. TSOP32 – 32 lead Plastic Thin Small Outline, 8 x 20mm, Package Mechanical Data**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.0472 |
| A1 | | 0.05 | 0.15 | | 0.0020 | 0.0059 |
| A2 | | 0.95 | 1.05 | | 0.0374 | 0.0413 |
| B | | 0.15 | 0.27 | | 0.0059 | 0.0106 |
| C | | 0.10 | 0.21 | | 0.0039 | 0.0083 |
| D | | 19.80 | 20.20 | | 0.7795 | 0.7953 |
| D1 | | 18.30 | 18.50 | | 0.7205 | 0.7283 |
| E | | 7.90 | 8.10 | | 0.3110 | 0.3189 |
| e | 0.50 | – | – | 0.0197 | – | – |
| L | | 0.50 | 0.70 | | 0.0197 | 0.0276 |
| α | | 0° | 5° | | 0° | 5° |
| N | 32 | | | 32 | | |
| CP | | | 0.10 | | | 0.0039 |

**Figure 12. TSOP32 – 32 lead Plastic Thin Small Outline, 8 x 20mm, Package Outline**




Note: Drawing is not to scale.

**Table 15. Revision History**

| Date | Rev. | Revision Details |
|---|---|---|
| July 1999 | -01 | First Issue |
| 28-Jul-2000 | -02 | New document template<br>Document type: from Preliminary Data to Data Sheet<br>Status Register bit DQ5 clarification<br>Data Polling Flowchart diagram change (Figure 4)<br>Data Toggle Flowchart diagram change (Figure 5)<br>Program/Erase Times specification change (Table 6)<br>$I_{CC1}$ and $I_{CC3}$ Typ. specification added (Table 10) |
| 22-Apr-2002 | -03 | PLCC32 package mechanical data modified |
| 19-Sep-2005 | 4.0 | PDIP32 package removed.<br>Table 14. Ordering Information Scheme: standard package added and ECOPACK version added for both standard package, and Tape & Reel packing. |

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